354 – Field-effect transistor (FET)

Acquired core competencies:

1. You understand the behavior of a controllable electrical component by means of parameterized characteristic curves.
2. You weigh the pros and cons of a high-impedance gate terminal.
3. You recognize the applicability of transistors in analog *and* digital circuits.

1 Tasks

1. Examine how an FET functions as a controllable resistor.
2. Set up an AC voltage amplifier using an FET. Vary the DC operating point and interpret your observations.
3. Analyze the high-impedance gate input of an FET using pre-specified circuits.
4. Estimate the gate capacitance of an FET experimentally.

2 Fundamentals

Keywords: charging & discharging a capacitor, current-based & voltage-based measurements

2.1 Field-effect transistors (FETs)

FETs are voltage-controlled devices. Applying a gate voltage U_{GS} can affect the conductivity of the drain-source channel. There are numerous types of FETs. In what follows, we will limit ourselves to the n-channel JFET, which is used here.

The JFET consists of an n-doped semiconductor crystal connected to a source (**S**) and a drain (**D**), see Fig. 1. The gate (**G**) is p-doped. At the interface between the p-region and the n-region, electrons (n→p) and holes (p→n) diffuse and recombine in the process. This creates a charge carrier depletion layer ( ). Therefore, the current between S and D can only flow along a channel, which is typical for FETs.

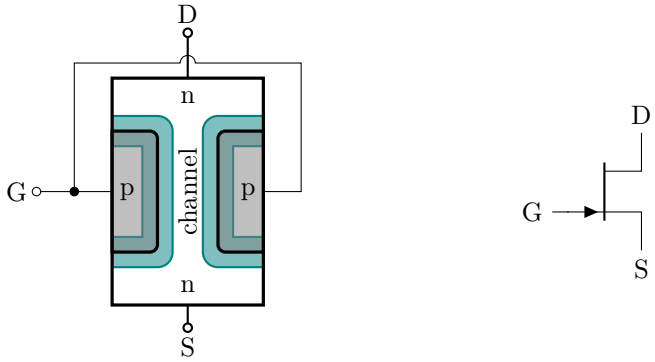


Figure 1: Schematic cross-section of an n-channel JFET. A barrier layer ( ) forms at the interface between the n-doped channel ( ) and the p-doped gate ( ). There are almost no free charge carriers in the barrier layer, which is why it is also called the charge carrier depletion layer. Right: JFET symbol used in circuit diagrams.

Applying a voltage U_{GS} between the gate and the source affects the extent of the depletion layer (▭). With the polarity shown in Fig. 2(b), the p-n junction between the gate and the channel behaves like a semiconductor diode in the backward direction (see Experiment 353), i.e., practically no current flows into the gate. The more negative the gate voltage becomes relative to the channel, the further the depletion region expands.

> The gate of an FET has a *very high impedance*, which means that FETs can be controlled *with virtually no current*.

The best channel conductivity (and thus the highest drain current I_D) occurs when $U_{GS} = 0\,V$. If the magnitude of U_{GS} is increased, the cross-sectional area of the channel decreases, and with it the current I_D, down to the extreme case of complete pinch-off (with $I_D = 0\,mA$).

Transistors, therefore, bear a certain resemblance to controllable resistors. However, unlike ohmic resistors, transistors have nonlinear $I(U)$ characteristics. Despite this – or perhaps precisely because of it – the two are compared in Fig. 2.

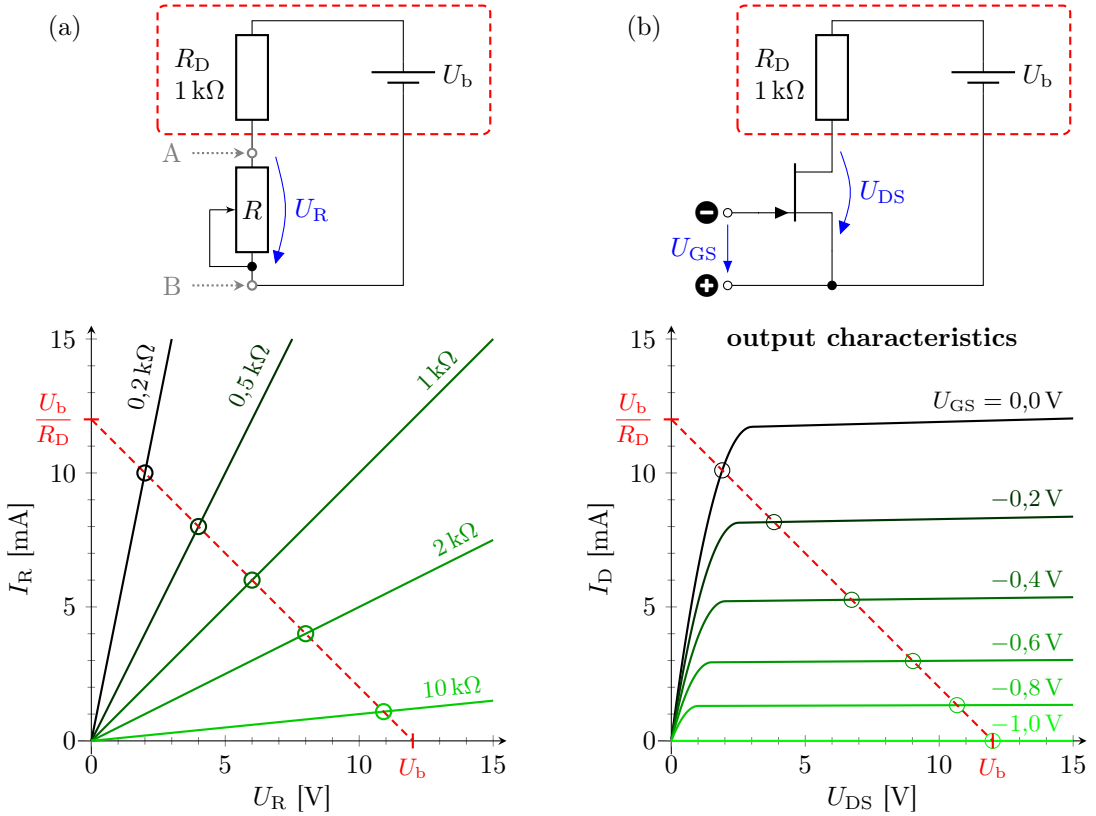


Figure 2: Comparison of (a) an adjustable resistive load and (b) a JFET. The basic circuit shown here is a **voltage divider** consisting of a voltage source U_b, a fixed resistor R_D, and a variable "resistor". The latter can be adjusted continuously over a wide range: In (a), R depends on the position of the slider; in (b), U_{GS} controls the channel conductivity. Only a finite selection of the $I(U)$ characteristic curves is shown in each case. U_b and R_D are combined into a practical source with an internal resistance, which is represented as a load line (red dashed line). The adjustable resistor and the JFET are passive components, which is why their $I(U)$ characteristics pass through the origin. Since the principle "current generated = current consumed" must hold, the circled graphical solution (operating point) is always determined by the intersection of the passive component's characteristic curve and the load line.

☞ Using Fig. 2(a), verify the correctness of the red dashed load line by conceptually removing the variable resistor and answering the following questions for the two resulting terminals, "A" and "B":

1. If you short-circuit A and B, how much current flows?
2. If you don't connect A and B but leave these terminals open, how large is the current?
3. How large is the voltage between A and B for each of the questions 1 and 2?
4. How large is the (absolute) slope of the load line and why?

The values for U_{GS} shown in Fig. 2(b) depend on the specific JFET model. Please note, therefore, that the JFET used in the Electronics lab may differ from these values.

But why should one use a transistor (*blend word:* **trans**fer res**istor**) instead of a variable resistor? In the case of the latter, the resistance is varied mechanically by means of a wiper, which can only operate at a limited speed. The inertia of the moving mass, as well as wear and tear, make high-frequency applications (MHz and above) impossible. Transistors, on the other hand, are electrically controlled and can therefore handle very high frequencies – depending on the type, up into the MHz and GHz ranges. The vacuum tubes, which were widely used in the first half of the 20th century and were also designed for high-frequency applications, were largely replaced by transistors, which can be manufactured in miniaturized form.

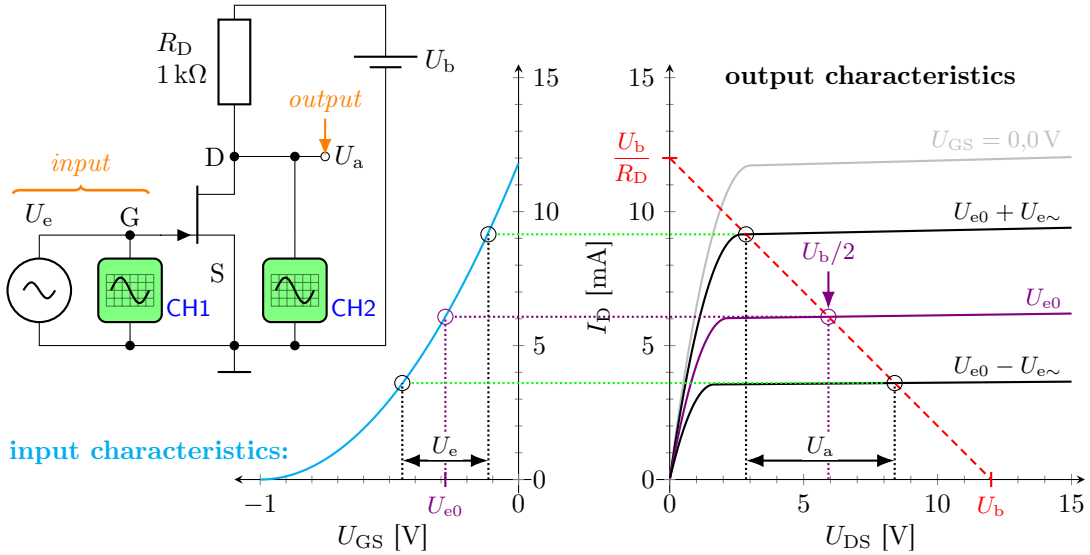


Figure 3: Same as Fig. 2(b), but here expanded to include a frequency generator at the input and an oscilloscope in two-channel mode (CH1 = input, CH2 = output). The DC offset U_{e0} of the frequency generator (*note the polarity!*) is set so that the DC operating point at the output lies at $U_{DS}(DC) = U_b/2$. An additional small AC voltage with amplitude $U_{e\sim}$ causes a dynamic oscillation of the operating point along the red dashed load line, indicated here by black circles for two values. At the output, an AC voltage is observed oscillating *nearly symmetrically* around $U_b/2$.

The controllability of the drain-source channel can be used to construct an AC voltage amplifier, see Fig. 6. At the gate input, a negative DC voltage $U_{e0} < 0\,V$ and an AC voltage signal are superimposed. The frequency generators used in the Electronics lab have independent adjustment options for both U_{e0} and the AC voltage amplitude $U_{e\sim}$. First, for $U_{e\sim} \to 0\,V_{AC}$, the value of U_{e0} is varied until the drain-source voltage U_{DS} is approximately $U_b/2$ (the "DC operating point" circled in purple in Fig. 3 → measure with a multimeter in DC mode!). Then the amplitude $U_{e\sim}$ is increased, causing the operating point to oscillate dynamically along the red dashed load line. Consequently, the drain-source voltage U_{DS} oscillates *almost symmetrically* around $U_b/2$. When using an oscilloscope, care must be taken to ensure that the output voltage

(circuit-imposed limits: $0\,\mathrm{V} < U_{\mathrm{DS}} \leq U_{\mathrm{b}}$) does not saturate, as the resulting distortion would significantly skew the gain measurement. If saturation occurs at the output, $U_{\mathrm{e}\sim}$ must be reduced accordingly. Small input signals $U_{\mathrm{e}\sim}$ produce significantly larger output signals $U_{\mathrm{a}\sim}$ with a voltage gain of $V_U = |U_{\mathrm{a}\sim}/U_{\mathrm{e}\sim}|$. The DC component at the output is generally of no interest and is therefore usually filtered out by a capacitor C_{a} located immediately before the output terminal. This capacitor blocks DC voltage, but allows AC voltage to pass through.

2.2 Charging and discharging of a capacitor

Like any p-n junction, the interface between the gate and the channel of a JFET also has a capacitance. The charge carrier depletion layer (▭), which is very poorly conductive, behaves like an insulating dielectric. On the two opposite sides of this dielectric layer are the n-doped region (▭) with negative charges and the p-doped region (▭) with positive charges. In essence, a p-n junction thus resembles a plate capacitor, which illustrates the presence of a capacitance. The higher this capacitance C, the slower the transistor responds to pulses at the gate, which makes it difficult to process high frequencies (compare the low-pass filter from Experiment 352). An estimate of the gate capacitance therefore provides insight into the maximum frequencies at which the transistor can be operated.

For the sake of simplicity, let us consider a standard plate capacitor here. If this capacitor is connected to a voltage source via a resistor, it will get charged. The time trace is described by an exponential relationship:

$$\text{charging:} \qquad U_{\mathrm{C}}(t) = U_0 \cdot \left(1 - e^{-t/\tau}\right) \tag{1}$$

Similarly, when the circuit is closed, the following relationship describes the discharging process:

$$\text{discharging:} \qquad U_{\mathrm{C}}(t) = U_0 \cdot e^{-t/\tau} \tag{2}$$

The characteristic time constant $\tau = RC$ is called the charging time. The greater the resistance and capacitance, the longer the charging and discharging take, see Fig. 4.

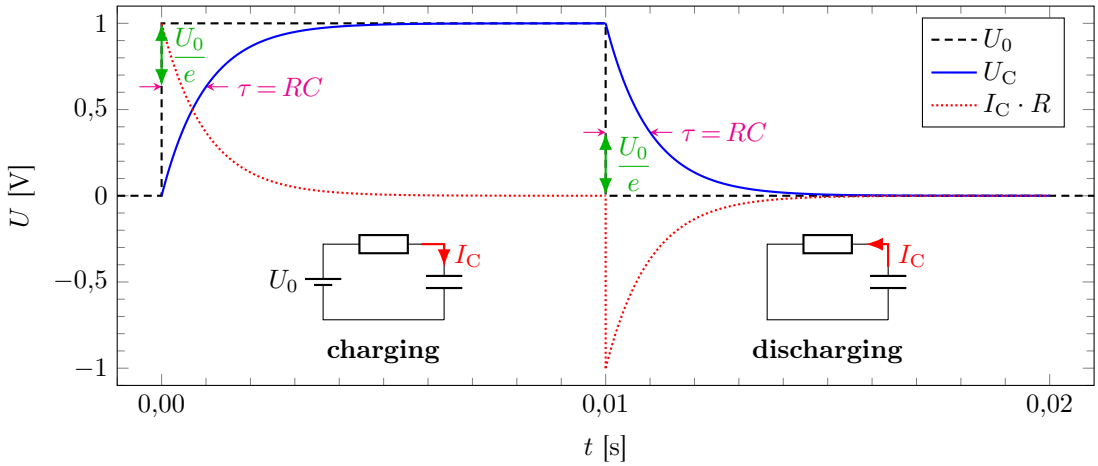


Figure 4: Charging and subsequent discharging behavior of an RC circuit, here with $R = 1\,\mathrm{k\Omega}$ and $C = 1\,\mu\mathrm{F}$. The current flow is calculated from the voltage drop across the capacitor $U_{\mathrm{C}}(t)$ as $I_{\mathrm{C}}(t) = C \cdot \mathrm{d}U_{\mathrm{C}}/\mathrm{d}t$, shown here as the product $I_{\mathrm{C}} \cdot R$.

In this experiment, we will determine the very small gate capacitance of a JFET by recording a discharge time trace. To accurately measure the characteristic time constant $\tau = RC$, we will therefore use a very large resistance of $1\,\mathrm{G\Omega}$.

3 Experimental procedure

1. *Controllability of the drain-source channel:* Set up the circuit shown in Fig. 5. Vary the gate-source voltage U_{GS} using a multiturn trimmer potentiometer and measure the drain-source voltage U_{DS} and the drain current I_D as a function of U_{GS}. Calculate the drain-source resistance $R_{DS} = U_{DS}/I_D$ for each value and plot both U_{DS} and R_{DS} against U_{GS}. Discuss your results in terms of current-based versus voltage-based measurements. 👉 In what voltage range is the relationship $U_{DS}(U_{GS})$ of your FET approximately linear? Such a linearity is advantageous for stable control. Discuss the role of the resistor R_D: For example, what would happen if R_D were allowed to approach zero? Furthermore, determine the minimum and maximum channel conductance $G_{DS} = I_D/U_{DS}$ (which is the reciprocal of R_{DS}) from your data.

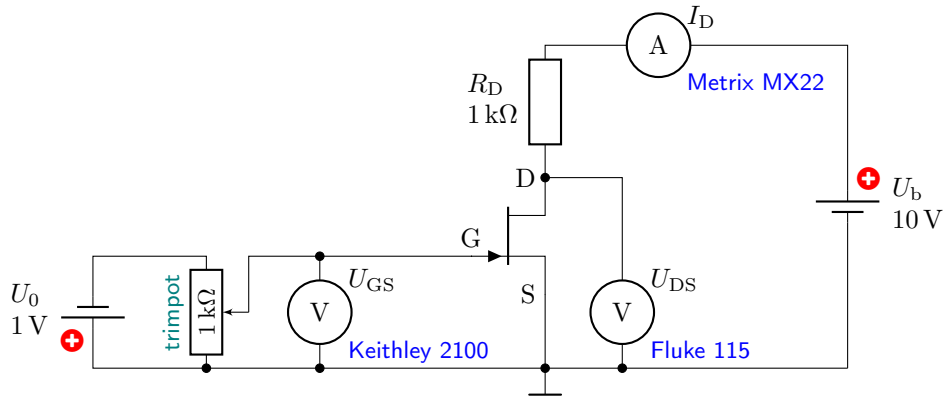


Figure 5: Investigation of the controllability of the drain-source channel. Use a 1 kΩ multiturn trimmer potentiometer (trimpot). Note the polarity of the sources! Explain in your report the choice of the specific measuring instruments made here.

2. *AC voltage amplifier:* Set up the circuit shown in Fig. 6.

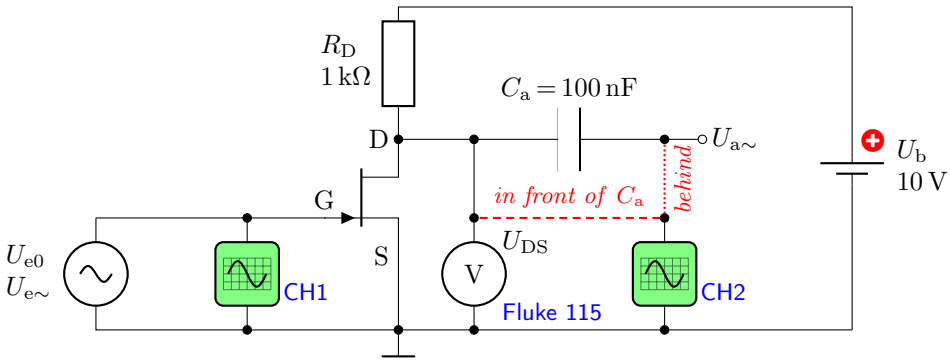


Figure 6: Circuit for amplifying small AC voltage signals using a JFET. The Fluke 115 digital multimeter must be operated in **DC mode**.

Adjusting the DC operating point: Using the offset control on the Hameg frequency generator (with 1×-20 dB attenuation and with the minimal AC amplitude setting), set a negative DC voltage $U_{e0} < 0$ V such that $U_{DS} = U_b/2 = 5\,V_{DC} \Rightarrow$ To do this, measure the DC voltage directly between drain (D) and source (S) with the digital multimeter, i.e., *in front of* the capacitor C_a. Now superimpose a sinusoidal voltage with $f = 10$ kHz from the same frequency generator and simultaneously record the input signal (CH1) and the output signal (CH2) with the oscilloscope in two-channel mode. Determine the maximum

input amplitude $U_{e\sim}$ at which no distortion of the sinusoidal signal $U_{a\sim}$ occurs at the output.

☞ How large is the voltage gain $V_U = |U_{a\sim}/U_{e\sim}|$?
☞ What is the role of the capacitor C_a? To answer this, record the output signals behind C_a (dotted line in Fig. 6) and in front of C_a (dashed line in Fig. 6) with the oscilloscope in **DC mode**.

3. *High-impedance input:* Set up the JFET circuit with the gate terminal open as depicted in Fig. 7(a). Display the output voltage on the oscilloscope in DC mode. Now touch the gate terminal. While doing this, stand up, move the sole of your shoe across the floor, and touch various potentials with your other hand – for example, the housing of a measuring device or a power supply cable. Describe your observations using appropriate oscilloscope recordings. How can you switch the state?
Now connect a light-emitting diode (LED) in series with the drain resistor R_D, as shown in Fig. 7(b). Touch the gate terminal again and observe the LED. Connect a short insulated wire to the gate. Then switch the LED back to its off state. Now touch the cable insulation and wait a few seconds. Discuss your observations.

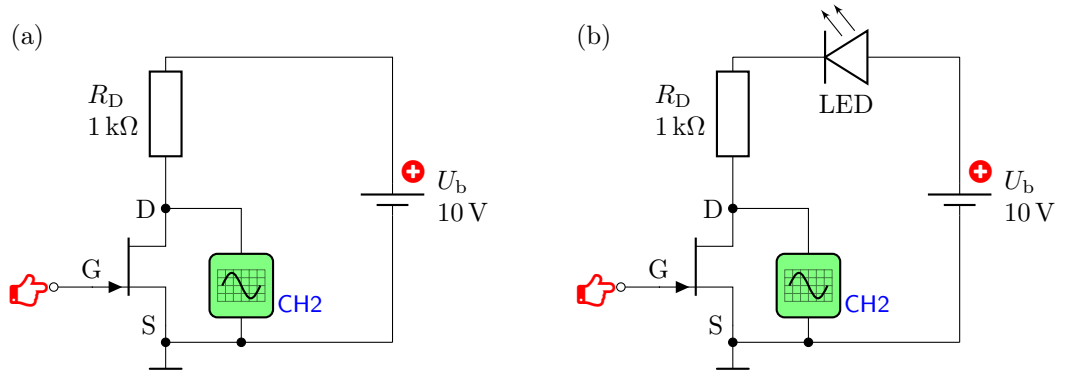


Figure 7: Circuits for demonstrating the high-impedance gate input. Use $U_b = 10\,V$ as the operating voltage. ☞ Touch the open gate.

4. Use a push-button to charge the *gate capacitance* and then discharge it through a 1 GΩ resistor, see Fig. 8. Record the discharge time trace $U_{DS}(t)$ on the drain-source channel using the oscilloscope's storage function (digital mode, single trigger, falling edge). Estimate the order of magnitude of the gate capacitance based on the $U_{DS}(t)$ curve.

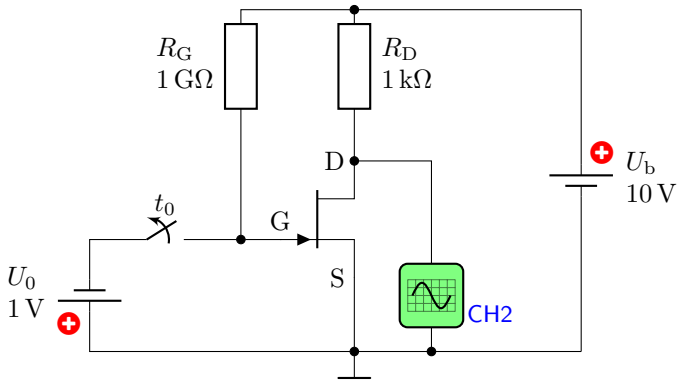


Figure 8: Circuit for determining the gate capacitance. The push-button is released at time t_0. The oscilloscope records the time trace of $U_{DS}(t)$ in digital mode.